SUDIP PAUDEL

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SUMMARY

Computer Engineering student at UT Arlington working across the stack — from bare-metal ARM firmware and FPGA RTL to deployed full-stack web apps. Experience writing register-level drivers, designing IEEE 754 arithmetic in SystemVerilog, and shipping two live AI platforms. Seeking a Summer 2026 engineering internship.

TECHNICAL SKILLS

- **Languages:** C, C++, SystemVerilog, Assembly (ARM), Java, JavaScript, SQL, HTML/CSS
- **Embedded / Hardware:** ARM Cortex-M4 (TM4C123), Intel MAX 10 FPGA, register-level drivers, timers & input capture, PWM, UART, interrupts (NVIC), static timing analysis, Raspberry Pi computer build
- **Tools:** TI Code Composer Studio, Intel Quartus Prime, Git, Linux, Next.js, React, Node.js, Supabase, OpenAI API, Vercel

PROJECTS

IR Remote Control Replacement — TM4C123GXL (ARM Cortex-M4) *Embedded Systems, UTA*

- Built a bare-metal universal IR remote that records and replays signals from any consumer remote via a UART command shell; wrote all drivers (clock, UART0, timers, NVIC) at the register level with no vendor HAL.
- Choose raw mark/space timing capture over protocol decoding (NEC/RC5/Sony), making the system remote-agnostic; captured edges with dual-edge input capture on Timer0A against a free-running 32-bit timestamp counter for microsecond resolution.
- Generated a 38 kHz carrier via Timer0B PWM, gated at runtime by switching a pin between GPIO and alternate-function; used SysTick-based gap detection for IR frame boundaries. Drove an IR emitter through a 2N3904 with a demodulating receiver.
- **Stack:** C, ARM Cortex-M4, TI Code Composer Studio

IEEE 754 Half-Precision Floating-Point Adder — FPGA *Digital Logic II, UTA*

- Designed and synthesized a 16-bit IEEE 754 floating-point adder/subtractor in SystemVerilog on an Intel MAX 10 FPGA, implementing operand magnitude ordering, exponent-difference mantissa alignment, sign-aware add/subtract, normalization, and overflow/underflow flags.
- Built the full user-facing system: a 4×4 matrix keypad scanner with FSM debounce and hex decoding, edge-detected operand capture, and a time-multiplexed 7-segment display driver.
- Synthesized to 706 logic elements / 137 registers; analyzed static timing results and identified the unrolled normalization shifter as the critical path, with pipelining as the route to closure.
- **Tools:** SystemVerilog, Intel Quartus Prime, static timing analysis

Network Security Project — Group Lead *UTA*

- Led a team designing and presenting a network security solution; coordinated task assignments and deadlines, and received faculty recognition for the team's contribution.

AntarLens — AI Cognitive Health Platform *antarlens.com*

- Built and deployed a full-stack AI platform that tracks focus, mood, energy, and sleep and predicts a user's cognitive patterns from their own data via a 30-second daily check-in.
- Architected the data model and auth with Supabase row-level security, isolating user records at the database layer; built a privacy-first design with encryption at rest and full user memory controls.
- **Stack:** Next.js, React, Supabase (Postgres, RLS), OpenAI API, Vercel

Kashlly — AI Financial Management Platform *kashlly.com*

- Built and deployed an AI financial tool for freelancers covering cash flow, invoicing, and runway forecasting, including a real-time runway calculator that converts financial data into plain-English guidance.
- Developed an AI pricing advisor that derives recommended rates from real expense data, and automated invoice follow-up that drafts and sends reminder emails on overdue invoices.

- **Stack:** Next.js, React, Supabase, OpenAI API, Vercel

EDUCATION

University of Texas at Arlington — B.E., Computer Engineering *Expected May 2027*

Relevant coursework: Digital Logic, Embedded Systems, Computer Architecture, Operating Systems, Electronics & Circuit Analysis, C Programming

Dallas College — Associate of Science *May 2024*

CERTIFICATIONS & ADDITIONAL

- **Certifications:** Google AI Essentials (Google); Ethical Hacking (Udemy).
- **Languages:** English, Nepali, Hindi (fluent). · Authorized to work in the U.S. · Available Summer 2026.